WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

a field area on the semiconductor substrate having a semiconductor insulating layer;

a plurality of active areas adjacent to the field area;

a first active area including a first FET (Field-Effect Transistor) and a second FET forming a circuit for outputting an output signal based on an input signal;

a second active area adjacent to the first active area across a field area on the side of the first FET;

a third active area adjacent to the first active area across a field area on the side of the second FET;

a fourth active area; and

a fifth active area adjacent to the fourth active area across a field area, wherein:

the difference between the distance between the first and second active areas and the distance between the first and third active areas is set smaller than the difference between the distance between the first and second active areas and the distance between the fourth and fifth active areas.

2. A semiconductor device comprising:

a semiconductor substrate;

a field area on the semiconductor substrate having a semiconductor insulating layer;

a plurality of active areas adjacent to the field area;

a first active area including a first FET and a second FET forming a circuit for receiving an input signal and outputting an output signal corresponding to the input signal;

a second active area adjacent to the first active area across a field area on the side of the first FET; and

a third active area adjacent to the first active area across a field area on the side of the second FET, wherein:

the distance between the first and second active areas is set equal within the extent of error to the distance between the first and second active areas.

3. A semiconductor device comprising:

a semiconductor substrate;

a field area on the semiconductor substrate having a semiconductor insulating layer;

a plurality of active areas adjacent to the field area;

a first active area including a first FET of n-type or p-type and a second FET of the same type forming a sense amplifier circuit to which at least two signals from a memory cell section are inputted via bit lines, the first and second FETs receiving the two

signals from the sense amplifier section;

a second active area adjacent to the first active area across a field area on the side of the first FET;

a third active area adjacent to the first active area across a field area on the side of the second FET;

a fourth active area; and

a fifth active area adjacent to the fourth active area across a field area, wherein:

the difference between the distance between the first and second active areas and the distance between the first and third active areas is set smaller than the difference between the distance between the first and second active areas and the distance between the fourth and fifth active areas.

4. A semiconductor device comprising:

a semiconductor substrate;

a field area on the semiconductor substrate having a semiconductor insulating layer;

a plurality of active areas adjacent to the field area;

a second active area adjacent to a first field area across the first field area;

a third active area in which a plurality of unit circuits are placed, the unit circuit including a first FET and a second FET and outputting an output signal based on an input signal;

a fourth active area adjacent to the third active area across a field area on the side of the first FETs; and

a fifth active area adjacent to the third active area across a field area on the side of the second FETs, wherein:

the distance between the third and fourth active areas or the distance between the third and fifth active areas is set longer than the distance between the first and second active areas.

5. A semiconductor device comprising:

a semiconductor substrate;

a field area on the semiconductor substrate having a semiconductor insulating layer;

a plurality of active areas surrounded by the field area;

a first FET and a second FET forming an electrically connected circuit having a function for outputting an output signal depending on an input signal;

a first active area in which the first FET is formed;

a second active area in which the second FET is formed;

a third active area adjacently located on a first side of the first active area across the field area;

a fourth active area adjacently located on a

second side of the first active area opposite to the first side across the field area;

a fifth active area adjacently located on the first side of the second active area across the field area;

a sixth active area adjacently located on the second side of the second active area opposite to the first side across the field area, wherein:

the difference between the distance between the first and third active areas and the distance between the second and fifth active areas or the difference between the distance between the first and fourth active areas and the distance between the second and sixth active areas is set smaller than the difference between the distance between the first and third active areas and the distance between the first and fourth active areas or the difference between the distance between the second and fifth active areas and the distance between the second and sixth active areas.

6. A semiconductor device comprising:

a semiconductor substrate;

a field area on the semiconductor substrate having a semiconductor insulating layer;

a plurality of active areas surrounded by the field area;

a first FET and a second FET forming a circuit having a first function;

a first active area in which the first FET is

formed;

a second active area in which the second FET is formed;

a third active area adjacently located on a first side of the first active area across the field area;

a fourth active area adjacently located on a second side of the first active area opposite to the first side across the field area;

a fifth active area adjacently located on the first side of the second active area across the field area;

a sixth active area adjacently located on the second side of the second active area opposite to the first side across the field area;

a seventh active area; and

an eighth active area adjacent to the seventh active area across the field area, wherein:

the difference between the distance between the first and third active areas and the distance between the second and fith active areas or the difference between the distance between the first and fourth active areas and the distance between the second and sixth active areas is set smaller than the difference between the distance between the first and third active areas and the distance between the seventh and eighth active areas.

7. A semiconductor device comprising:

a semiconductor substrate;

a memory cell section on the semiconductor substrate; and

a sense amplifier section on the semiconductor substrate which is electrically connected with the memory cell section via bit lines, wherein:

each of the memory cell section and the sense amplifier section includes a field area having a semiconductor insulating layer and a plurality of active areas adjacent to the field area each of which including a plurality of FETs arranged therein, and

the distance between the edge of the first active area and an FET in the first active area nearest to the edge is set to three times or more of the distance between a first FET in the first active area and a second FET in the first active area nearest to the first FET.

8. A semiconductor device comprising:

a semiconductor substrate;

a field area on the semiconductor substrate having a semiconductor insulating layer;

a plurality of active areas surrounded by the field area;

a first active area in which a first n-type FET and a second n-type FET are formed;

a second active area in which a first p-type FET and a second p-type FET are formed;

a circuit including the first and second n-

type FETs and the first and second p-type FETs and being electrically connected with a memory cell section, the circuit at least receiving a first input signal from the memory cell section with the first and second n-type FETs, receiving a second input signal from the memory cell section with the first and second p-type FETs, and outputting an output signal based on the input signals;

a third active area which is formed adjacent to the first active area across a field area on the side of the first n-type FET;

a fourth active area which is formed adjacent to the first active area across a field area on the side of the second n-type FET;

a fifth active area which is formed adjacent to the second active area across a field area on the side of the first p-type FET; and

a sixth active area which is formed adjacent to the second active area across a field area on the side of the second p-type FET, wherein:

the difference between the distance between the first and third active areas and the distance between the first and fourth active areas or the difference between the distance between the second and fifth active areas and the distance between the second and sixth active areas is set smaller than the difference between the distance between the first and third active areas and the distance between the second

and fifth active areas.

9. A semiconductor device comprising:

a semiconductor substrate;

a field area on the semiconductor substrate having a semiconductor insulating layer;

a plurality of active areas adjacent to the field area;

a first active area including a first FET and a second FET forming a circuit for outputting an output signal based on an input signal;

a second active area adjacent to the first active area across a field area on the side of the first FET;

a third active area adjacent to the first active area across a field area on the side of the second FET;

a third FET formed in an active area of a memory cell which is formed on the semiconductor substrate; and

a fourth FET placed adjacent to the third FET, wherein:

the difference between threshold voltages of the first and second FETs is set smaller than the difference between threshold voltages of the third and fourth FETs.

10. The semiconductor device as claimed in claim 1, wherein gate length of at least one of the FETs is 0.25μm or less.

11. The semiconductor device as claimed in claim 1, wherein the circuit is one selected from a differential amplifier circuit, a current mirror circuit, a switched capacitor circuit and a constant current/voltage circuit.

12. A method for manufacturing a semiconductor device, comprising the steps of:

a step for forming a field area having a semiconductor insulating layer on a semiconductor substrate and forming at least first through fifth active areas which are arranged adjacently via the field area;

a step for forming a first FET in part of the first active area on the side of the second active area and forming a second FET in part of the first active area on the side of the third active area; and

a step for forming a circuit including the first and second FETs which outputs an output signal based on an input signal, wherein:

the difference between the distance between the first and second active areas and the distance between the first and third active areas is set smaller than the difference between the distance between the first and second active areas and the distance between the fourth and fifth active areas.

13. A method for manufacturing a semiconductor device, comprising the steps of:

a step for forming a field area having a

semiconductor insulating layer on a semiconductor substrate and forming at least first through sixth active areas which are arranged adjacently via the field area, in which the third active area adjacently located on a first side of the first active area across the field area, the fourth active area adjacently located on a second side of the first active area opposite to the first side across the field area, the fifth active area adjacently located on the first side of the second active area across the field area, and the sixth active area adjacently located on the second side of the second active area opposite to the first side across the field area are formed;

a step for forming a first FET in the first active area and forming a second FET in the second active area; and

a step for forming a circuit including the first and second FETs which outputs an output signal based on an input signal, wherein:

the difference between the distance between the first and third active areas and the distance between the second and fifth active areas or the difference between the distance between the first and fourth active areas and the distance between the second and sixth active areas is set smaller than the difference between the distance between the first and third active areas and the distance between the first and fourth active areas or the difference between the

distance between the second and fifth active areas and the distance between the second and sixth active areas.

14. A method for manufacturing a semiconductor device, comprising the steps of:

a step for forming a field area having a semiconductor insulating layer on a semiconductor substrate and forming at least first through eighth active areas which are arranged adjacently via the field area, in which the third active area adjacently located on a first side of the first active area across the field area, the fourth active area adjacently located on a second side of the first active area opposite to the first side across the field area, the fifth active area adjacently located on the first side of the second active area across the field area, the sixth active area adjacently located on the second side of the second active area opposite to the first side across the field area, the seventh active area, and the eighth active area adjacent to the seventh active area across the field area are formed;

a step for forming the first FET in the first active area and forming the second FET in the second active area; and

a step for forming the circuit including the first and second FETs which outputs an output signal based on an input signal, wherein:

the difference between the distance between the first and third active areas and the distance

between the second and fifth active areas or the difference between the distance between the first and fourth active areas and the distance between the second and sixth active areas is set smaller than the difference between the distance between the first and third active areas and the distance between the seventh and eighth active areas.

15. A method for manufacturing a semiconductor device, comprising the steps of:

a step for forming a field area having a semiconductor insulating layer on a semiconductor substrate and forming a plurality of active areas adjacent to the field area;

a step for forming a plurality of FETs in a first active areas; and

a step for forming a memory cell section and forming a sense amplifier section including the first and second FETs which is electrically connected with the memory cell section via bit lines, wherein:

the distance between the edge of the first active area and an FET in the first active area nearest to the edge is set to three times or more of the distance between a first FET in the first active area and a second FET in the first active area nearest to the first FET.